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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,054	01/30/2004	Yuichi Okuda	501.43354X00	5473

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EXAMINER	
MERANT, GUERRIER	
ART UNIT	**PAPER NUMBER.**
2138	

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,054	OKUDA, YUICHI	
	Examiner	Art Unit	
	Guerrier Merant	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 01/30/04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 20040130.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is the initial office action based on the application filed on January 30, 2004. Claims 1-9 are currently pending and have been considered below.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

Claims 1, 2, 6, and 7 recite the limitation "***x+1 bits***" in the third paragraph of claims 1 and 6, also the last two lines of claims 2 and 7. There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

2. Claims 3, 5 and 8 are objected to because of the following informalities:

In the first paragraph of claims 3 and 8, the Examiner is unclear the **"input/output"** is **"input or output"** or **"input and output"**. Appropriate correction is required.

In the third paragraph of claim 5, The Examiner is unclear is **"the storing location"** is referring to **"the information storing part"**. Also, The Examiner believes that **"...information code is allocated to the position..."** should be **"...information code is allocated to a position..."** Appropriate correction is required.

3. According to the Examiner's interpretation, Claims 1-4 and 6-9 are rejected in light of the 35 U.S.C 112 second paragraph rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 & 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by **Sonobe (US 6,295,617)**.

Claims 1 and 6: **Sonobe** discloses a test method of semiconductor memory device or a semiconductor memory device *(Fig. 1)* comprising:

a) an information storing part *(items 1 & 4; Fig. 1)* for storing an m-bit information code and an n-bit check code for one piece of position information *(col. 6, lines 62-67 & col. 7, lines 1-13)*;

b) an ECC circuit capable *(item 7; Fig. 1)* of correcting, from an information code and a check code stored in said information storing part, an error of said information code to x bits *(col. 5, lines 31-37; col. 6, lines 30-37 & col. 7, lines 26-36)* ;

c) and a parallel test circuit *(item 8; Fig. 1)* for receiving an information code and a check code for test with the same bits stored in said information

storing part and deciding a defect with x+1 bits or more for one piece of position information as being defective *(col. 5, lines 1-17; col. 6, lines 45-59 & col. 7, lines 42-47)*.

Claims 2 and 7: **Sonobe** discloses a test method of semiconductor memory device or a semiconductor memory device *(Fig. 1)* as in claims 1 and 6 above, wherein a plurality of said information storing parts are accessible individually *(col. 2, lines 3-13)*, wherein a plurality of said parallel test circuits are provided corresponding to said plurality of information storing parts, respectively, wherein said ECC circuit is provided to be shared among said plurality of information storing parts *(col. 7, lines 54-67 & col. 8, lines 1-20)*, and wherein said plurality of information storing parts store an information code and a check code for test in the same pattern, said plurality of parallel test circuits are valid in parallel in test mode, each deciding a defect with x+1 bits or more as being defective for outputting individually *(col. 5, lines 38-63)*.

Claims 3 and 8: **Sonobe** discloses a test method of semiconductor memory device or a semiconductor memory device *(Fig. 1)* as in claims 1 and 6 above, further comprising: a z-bit information input/output terminal in which the relation of z>n is established *(wD1-WD8 & TD1-TD4)*; and a write signal path in which at information input in test mode, an information input terminal with n bits of z bits is used to be written as an n-bit check code into said information storing part and

an information input/output terminal with the remaining z-n bits or less is used to be written thereinto as an information code of said information storing part *(col. 9, lines 48-67 & col. 10, lines 1-19)*.

Claims 4 and 9: **Sonobe** discloses a test method of semiconductor memory device or a semiconductor memory device *(Fig. 1)* as in claims 3 and 8 above, further comprising a read path in which an information code and a check code stored in said information storing part are used for reading in test mode (corresponding to allocation of said information code and check code to the information input/output terminal, used at said information input in test mode *(col. 7, lines 25-36 & col. 8, lines 7-33)*.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonobe** and further in view of **Jeddeloh et al (US 5,430,742).**

Claim 5: **Sonobe** discloses a semiconductor memory device *(Fig. 1)* comprising: a) an information storing part *(items 1 & 4; Fig. 1)* for storing an m-bit information code and an n-bit check code for one piece of position information *(col. 6, lines 62-67 & col. 7, lines 1-13)*;

b) an ECC circuit capable *(item 7; Fig. 1)* of correcting, from an information code and a check code stored in said information storing part, an error of said information code to x bits *(col. 5, lines 31-37; col. 6, lines 30-37 & col. 7, lines 26-36)*. But **Sonobe** fails to disclose the storing location of said information code is allocated to the position capable of inputting and outputting information faster than the storing location of said check code. However, **Jeddeloh et al.** discloses a memory controller with ecc and data stream control, wherein "page mode" is use to speed up the memory access. *Page mode is a fast memory transfer for a large segment of data. One page mode memory access can typically be completed within 100 nanoseconds. In page mode, the row address select (RAS) input to the DRAMs is held active while the column address select (CAS) for the DRAMs is used to clock the proper address into the memory. Since the amount of set-up time required between CAS signals is relatively short, a memory transfer which involves consecutive memory segments can be accomplished quickly using DRAMs operating in page mode (col. 3, lines 9-19).* Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to incorporate in the information storing part *(items 1 & 4; Fig. 1) of*

Sonobe the "page mode" process of **Jeddeloh et al.** in order to minimize time while testing the device.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a) **Zulian (US 4,862,462)** discloses a memory systems and related error detection and correction apparatus.

b) **Wu et al. (US 5,912,906)** discloses a method and apparatus for recovering from correctable ecc errors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (571) 272-3819. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Merant Guerrier
11/29/06

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